**Introduction to ModelSim**

**LAB # 09**

****

**Fall 2021**

**CSE304L Computer Organization & Architecture**

Submitted by: **Ashfaq Ahmad**

Registration No: **19PWCSE1795**

Class Section: **B**

Student Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

**Prof: Ammad khalil**

February 13, 2022

**Department of Computer Systems Engineering**

**University of Engineering and Technology, Peshawar**

**Objective:**

* To know about Modelsim.
* How it install.
* What is VHDL and verilog
* How to compile and simulate verilog code.

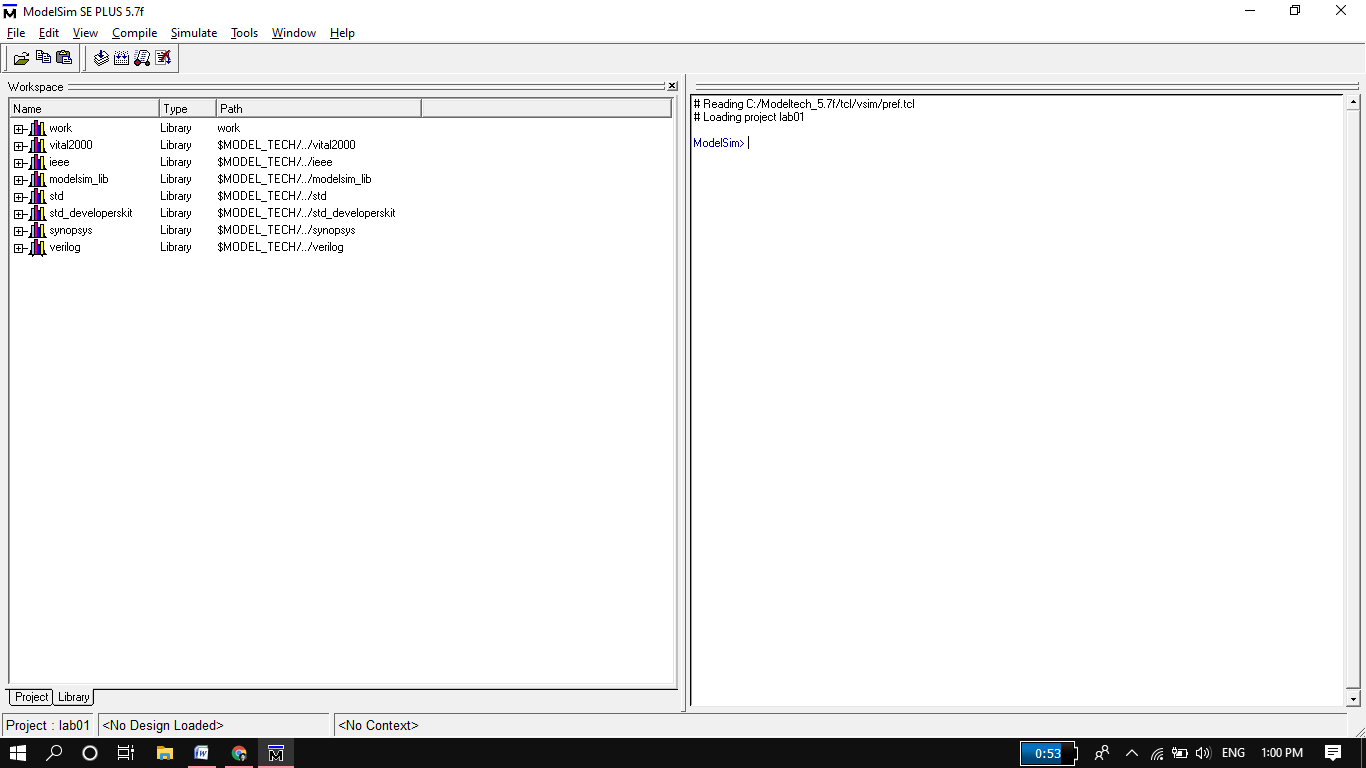
**ModelSim:**

* ModelSim is a program created by Mentor Graphics used for simulation of VHDL and Verilog designs.
* ModelSim is a Hardware Descriptive Language (HDL) simulation environment for simulation of various languages such as VHDL, Verilog and SystemC, and includes a built-in C debugger.
* It is the most widely use simulation program in business and education.

**Steps of installation:**

1. Unzip, unRAR or use the installer
2. Install using "setup.exe"
3. After installation, copy "mgls.dll", "modeltech.exe" and "vlm.exe" into your "\Win32" dir, overwrite when prompted
4. Copy "license.dat" into your "\Win32" dir and into "C:\FlexLM", overwrite when prompted.
5. Done

**Interface of Modelsim:**



**How to use ModelSim?**

**Step 1**

**Create a new project:**

Select **File > New > Project** (Main window) to create a new project. This opens the **Create Project dialog**. The dialog includes these options:

* **Project Name:**

The name of the new project.

* **Project Location:**

The directory in which the .mpf file will be created.

* **Default Library Name:**

The name of the working library.

You can generally leave the **Default Library Name** set to "work." The name you specify will be used to create a working library subdirectory within the Project Location. After selecting OK, you will see a blank Project tab in the workspace area of the Main window and the **Add Items to the Project** dialog.

**Step 2**

**Adding items to the project:**

The **Add Items to the** **Project dialog** includes these options:

* **Create New File:**

Create a new VHDL, Verilog, Tcl, or text file using the Source window. See below for details.

* **Add Existing File:**

Add an existing file. See below for details.

* **Create Simulation:**

Create a Simulation Configuration that specifies source files and simulator options.

* **Create New Folder:**

Create an organization folder.

* **Create New File:**

The **Create New File** command lets you create a new VHDL, Verilog, Tcl, or text file using the Source window. You can also access this command by selecting File > Add to Project > New File (Main window) or right-clicking (2nd button in Windows; 3rd button in UNIX) in the Project tab and selecting Add to Project > New File.

* **The Create Project File:**

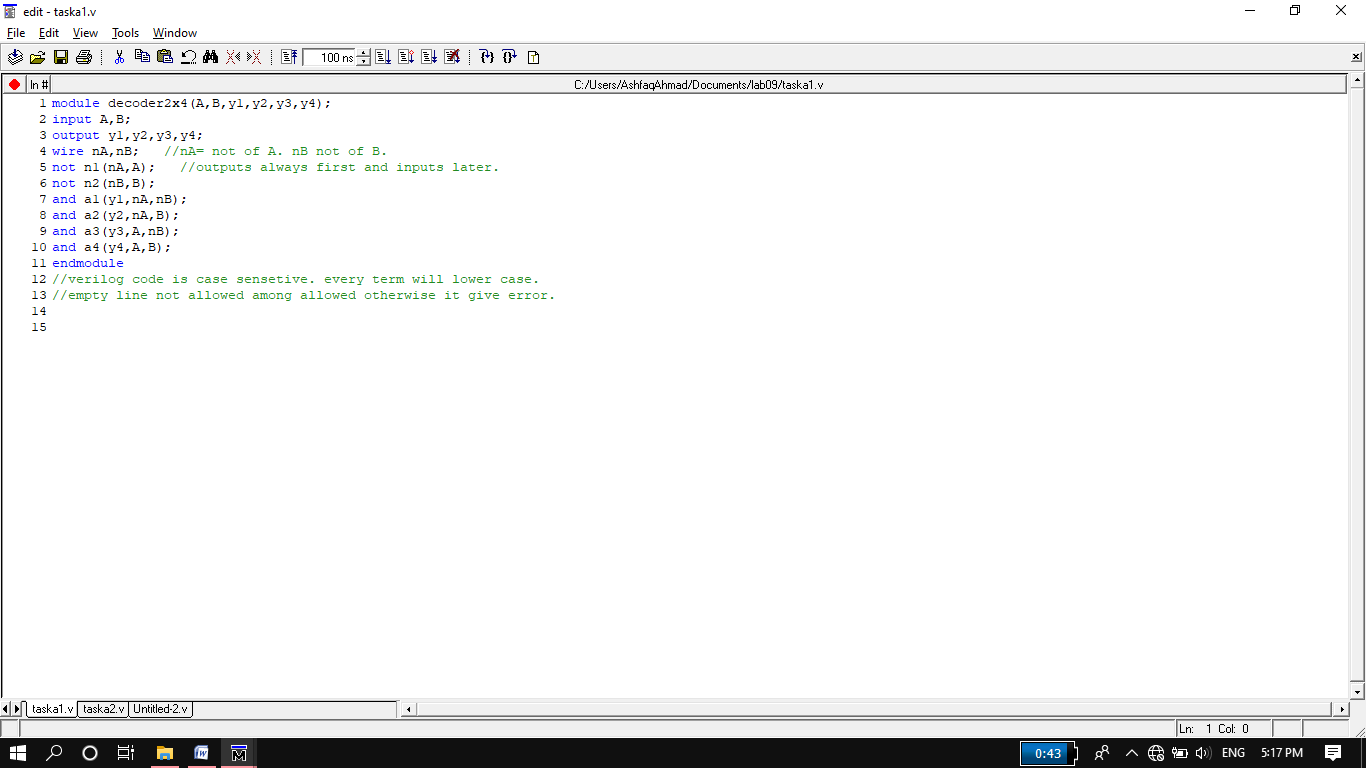
Dialog includes these options:

* **File Name:** The name of the new file
* **Add file as type:** Add the type of the new file. Select VHDL, Verilog, TCL, or text.
* **Folder:**  The organization folder in which you want the new file placed. You must first create folders in order to access them here.

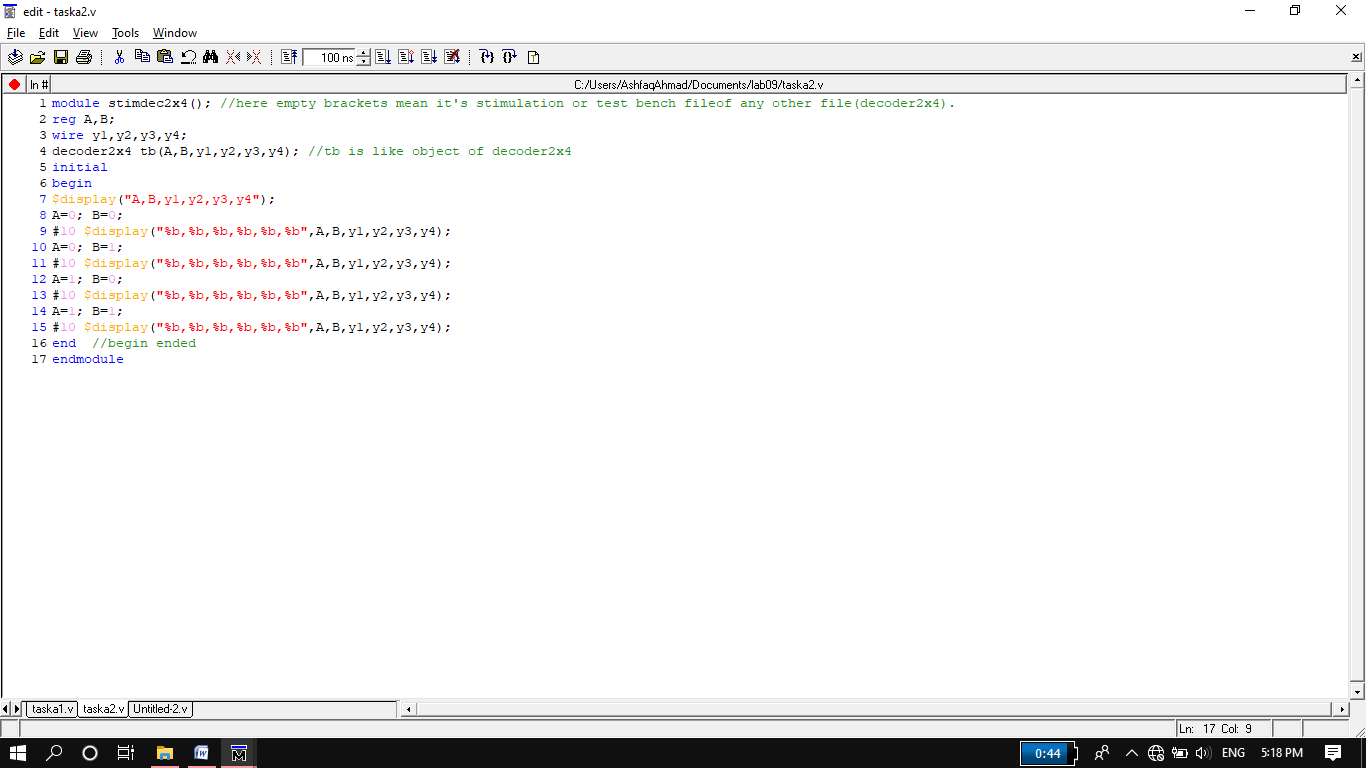
When you select OK, the Source window opens with an empty file, and the file is listed in the Project tab of the Main window workspace.

**Task01: 2x4 Decoder**

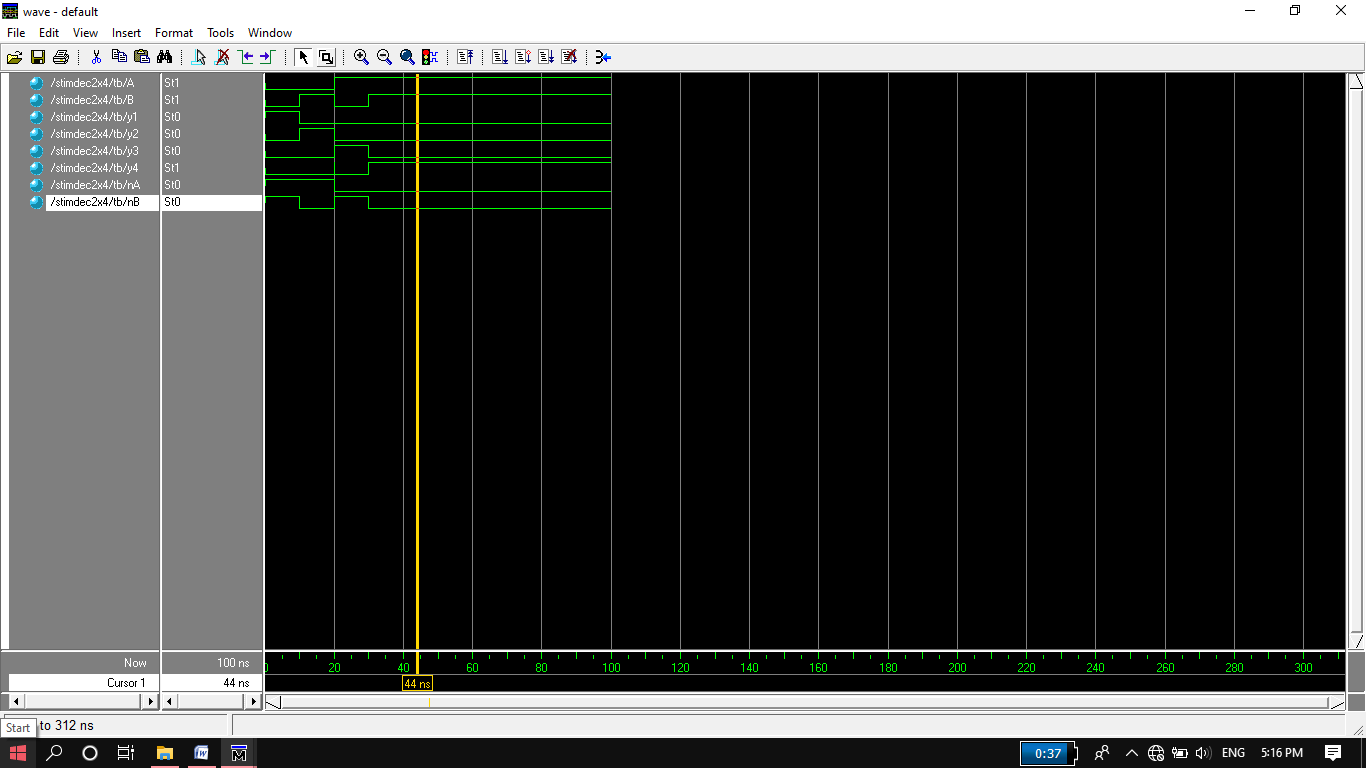
**Logic code:**



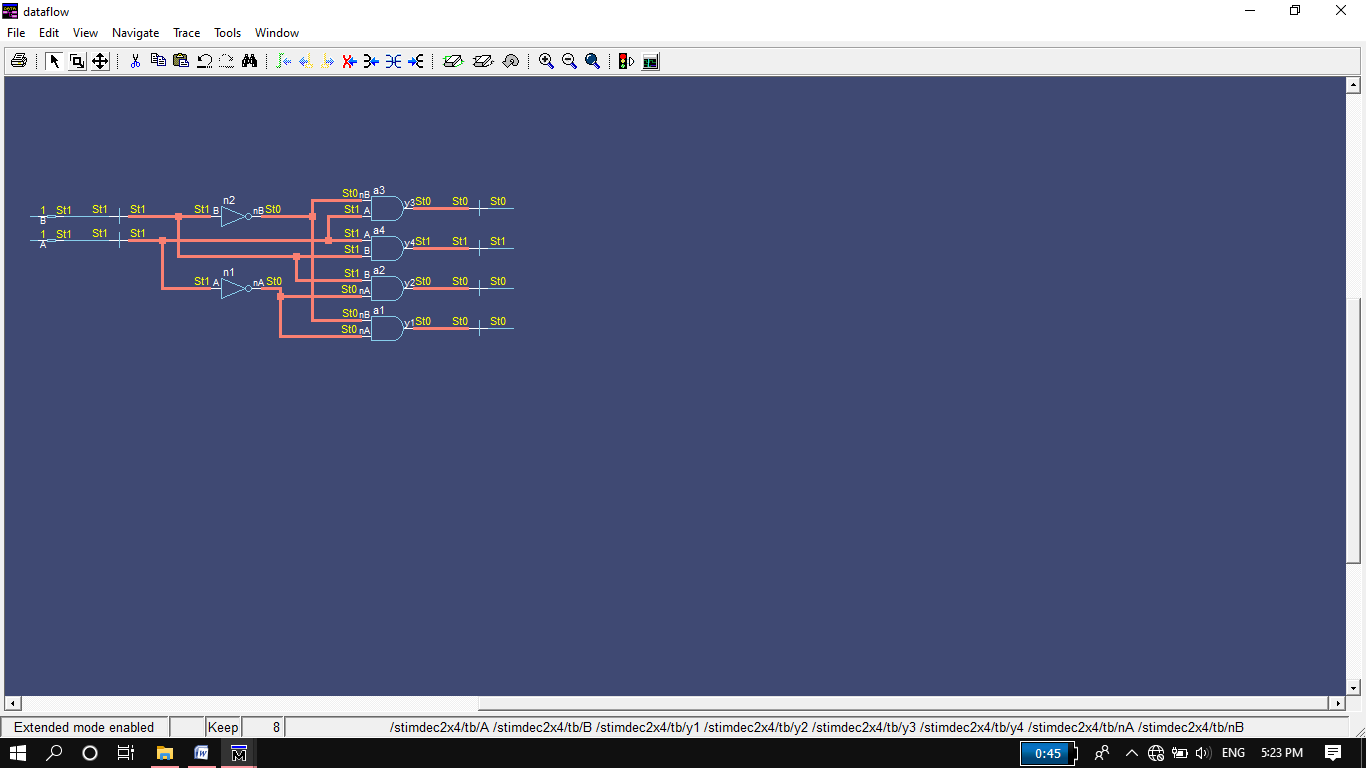
**Test bench:**



**Wave Output:**

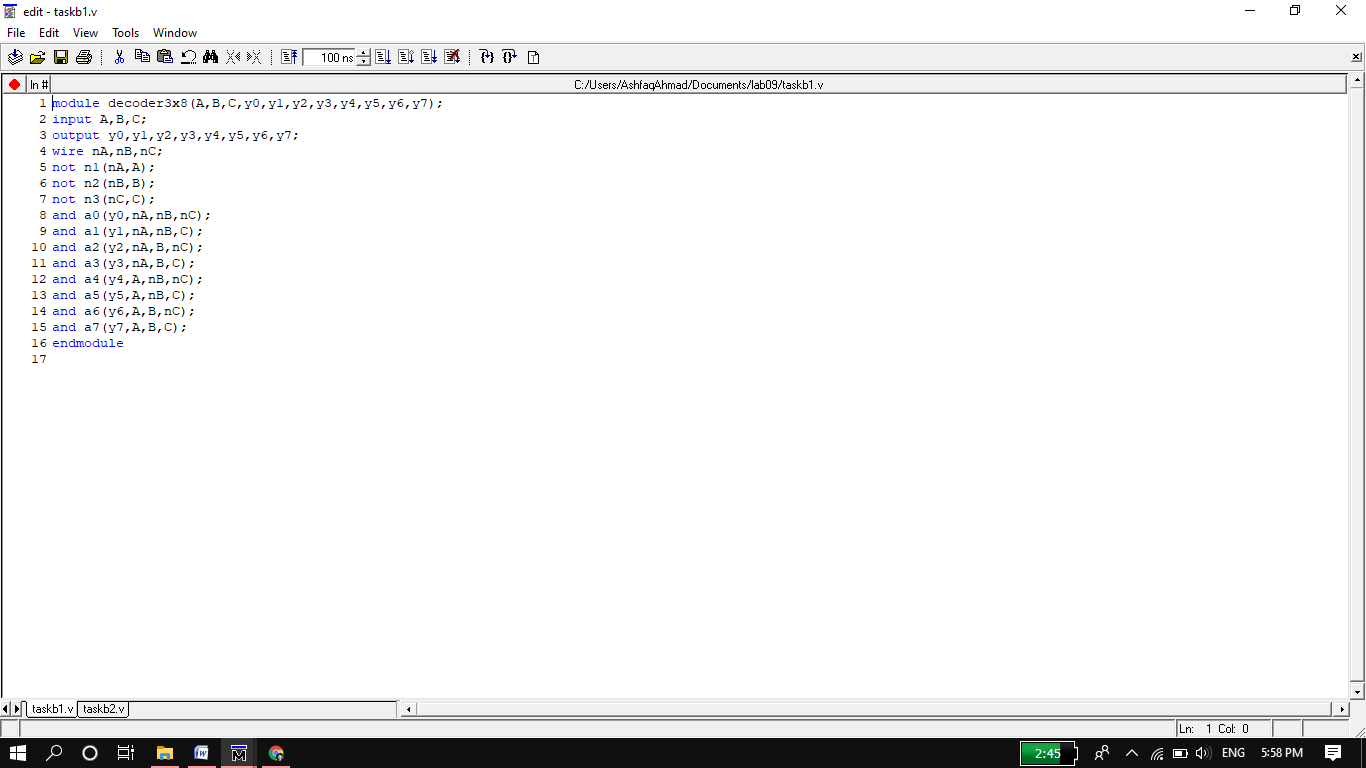


**Circuit:**

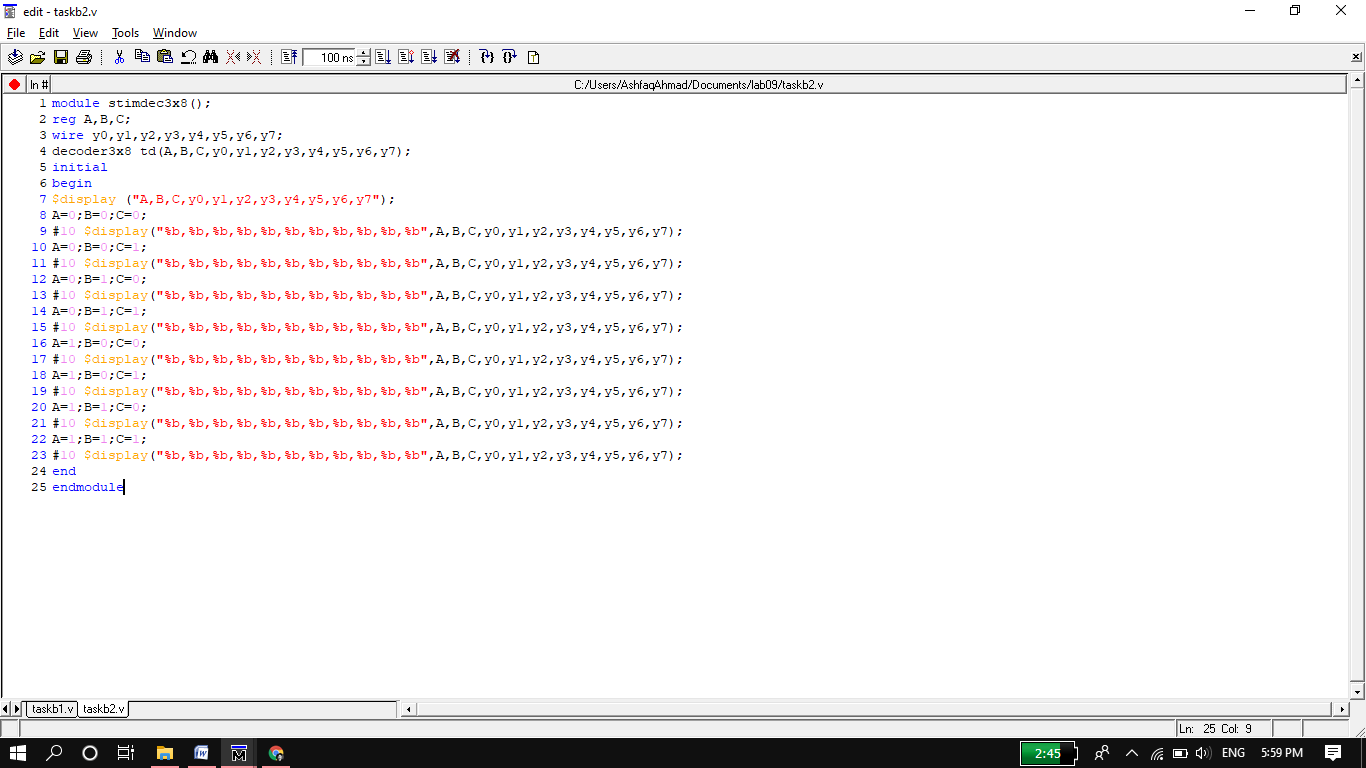


**Task01: 3x8 Decoder**

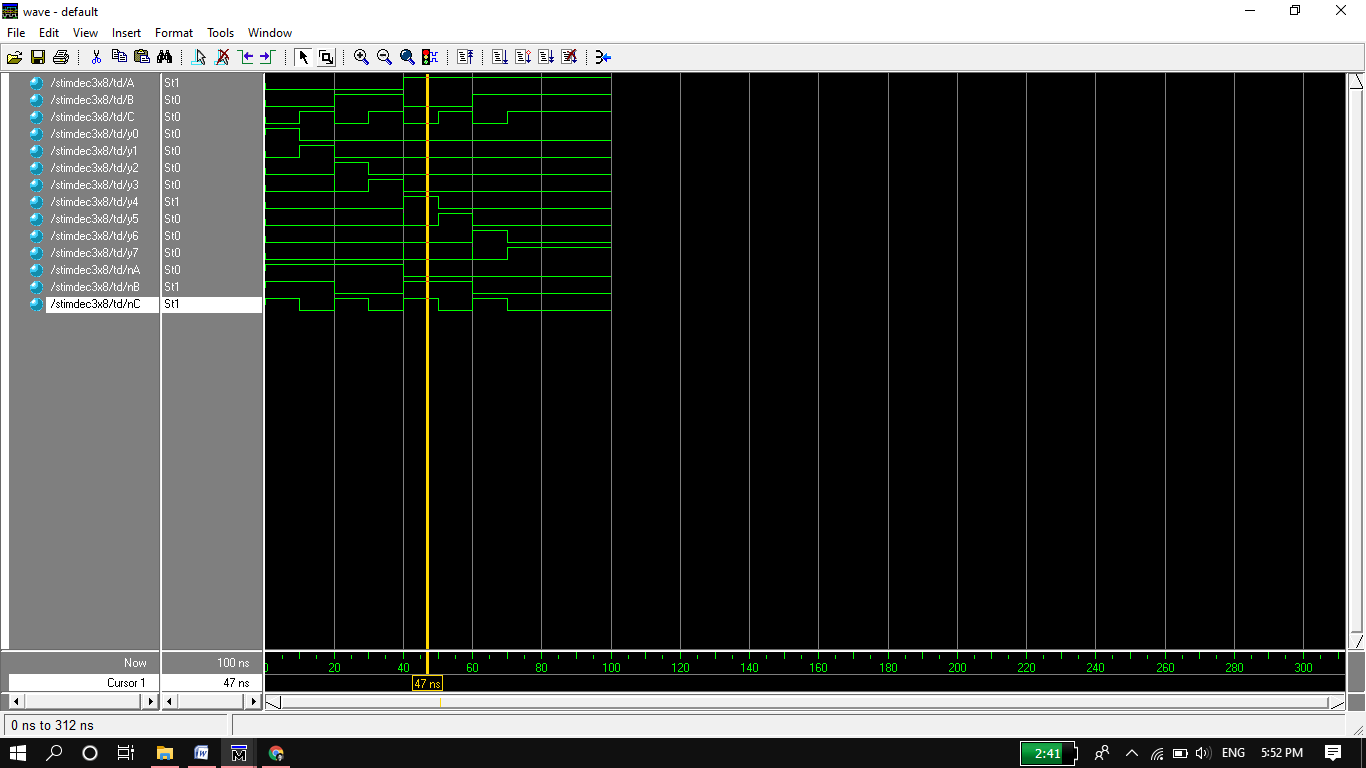
**Logic code:**



**Test bench:**



**Wave Output:**



**Circuit:**

